36-V, Single-Supply, 10-MHz, Rail-to-Rail Output Operational Amplifiers

Check for Samples: OPA172, OPA2172, OPA4172

FEATURES

- **Wide Supply Range: +4.5 V to +36 V, ±2.25 V to ±18 V**
- **Low Offset Voltage: ±0.2 mV**
- **Low Offset Drift: ±0.3 µV/°C**
- **Gain Bandwidth: 10 MHz**
- **Low Input Bias Current: ±8 pA**
- **Low Quiescent Current: 1.6 mA per Amplifier**
- **Low Noise: 6 nV/√Hz**
- **EMI and RFI Filtered Inputs**
- **Input Range Includes the Negative Supply**
- **Input Range Operates to Positive Supply**
- **Rail-to-Rail Output**
- **High Common-Mode Rejection: 120 dB**
- **Industry-Standard Packages:**
  - **8-Pin SOIC**
  - **8-Pin MSOP**
  - **14-Pin SOIC**
  - **14-Pin TSSOP**
- ***micro*Packages:**
  - **Single in SC-70, SOT-23**

APPLICATIONS

- **Tracking Amplifier in Power Modules**
- **Merchant Power Supplies**
- **Transducer Amplifiers**
- **Bridge Amplifiers**
- **Temperature Measurements**
- **Strain Gauge Amplifiers**
- **Precision Integrators**
- **Battery-Powered Instruments**
- **Test Equipment**

DESCRIPTION

The OPA172, OPA2172 and OPA4172 (OPAx172) are a family of 36-V, single-supply, low-noise operational amplifiers with the ability to operate on supplies ranging from +4.5 V (±2.25 V) to +36 V (±18 V). This latest addition of high voltage CMOS operational amplifiers, in conjunction with the OPAx171 and OPAx170 provide a family of bandwidth, noise, and power options to meet the needs of a wide variety of applications. The OPAx172 are available in micropackages and offer low offset, drift, and quiescent current. These devices also offer wide bandwidth, fast slew rate, and high output current drive capability. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

Unlike most op amps, which are specified at only one supply voltage, the OPAx172 family is specified from +4.5 V to +36 V. Input signals beyond the supply rails do not cause phase reversal. The input can operate 100 mV below the negative rail and within 2 V of the top rail during normal operation. Note that these devices can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail.

The OPAx172 series of op amps are specified from –40°C to +125°C.

PRODUCT FAMILY

DEVICE	PACKAGE
OPA172 (single)(1)	SC-70, SOT23-5, SO-8
OPA2172 (dual)	SO-8, MSOP-8
OPA4172 (quad)	TSSOP-14, SO-14

AMPLIFIER SELECTION TABLE

DEVICE	QUIESCENT CURRENT (I_Q)	GAIN BANDWIDTH (GBW)	VOLTAGE NOISE DENSITY (e_n)
OPAx172	1600 µA	10 MHz	6 nV/√Hz
OPAx171	475 µA	3.0 MHz	14 nV/√Hz
OPAx170	110 µA	1.2 MHz	19 nV/√Hz

(1) OPA172 SO-8 package is production data. All other devices are product preview.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

			VALUE	UNIT
Supply voltage			±20 (+40 single supply)	V
Signal input terminals	Voltage(2)	Common-mode	(V–) – 0.5 to (V+) + 0.5	V
		Differential	±0.5	V
	Current		±10	mA
Output short circuit(3)			Continuous	
Operating temperature			–55 to +150	°C
Storage temperature			–65 to +150	°C
Junction temperature			+150	°C
Electrostatic discharge (ESD) ratings:	Human body model (HBM)		4	kV
	Charged device model (CDM)		1	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Transient conditions that exceed these voltage ratings should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±2.25 V to ±18 V, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±0.2	±1	mV
	Over temperature	T_A = –40°C to +125°C			±1.15	mV
dV_{OS}/dT	Drift	T_A = –40°C to +125°C		±0.3	±1.5	µV/°C
PSRR	vs power supply	T_A = –40°C to +125°C		±1	±3	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±8	±15	pA
	Over temperature	T_A = –40°C to +125°C			±14	nA
I_{OS}	Input offset current			±2	±15	pA
	Over temperature	T_A = –40°C to +125°C			±1	nA
NOISE						
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz		1.2		μV_{PP}
e_n	Input voltage noise density	f = 100 Hz		8.6		$nV/\sqrt{Hz}$
		f = 1 kHz		6		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1 kHz		1.6		$fA/\sqrt{Hz}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range(1)		(V–) – 0.1 V		(V+) – 2 V	V
CMRR	Common-mode rejection ratio	V_S = ±2.25 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_A = –40°C to +125°C	90	104		dB
		V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_A = –40°C to +125°C	110	120		dB
INPUT IMPEDANCE						
	Differential			100 || 4		MΩ || pF
	Common-mode			6 || 4		10^{13}Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.35 V < V_O < (V+) – 0.35 V, R_L = 10 kΩ, T_A = –40°C to +125°C	110	130		dB
		(V–) + 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ, T_A = –40°C to +125°C		116		dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product			10		MHz
SR	Slew rate	G = +1		10		V/µs
t_S	Settling time	To 0.1%, V_S = ±18 V, G = +1, 10-V step		2		µs
		To 0.01% (12 bit), V_S = ±18 V, G = +1, 10-V step		3.2		µs
	Overload recovery time	V_{IN} × Gain > V_S		200		ns
THD+N	Total harmonic distortion + noise	V_S = +36 V, G = +1, f = 1 kHz, V_O = 3.5 V_{RMS}		0.00005		%

(1) The input range can be extended beyond (V+) – 2 V up to (V+) + 0.1 V. See the *Typical Characteristics* and *Application Information* sections for additional information.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±2.25 V to ±18 V, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output swing from rail	V_S = +36 V	R_L = 10 kΩ		75	80	mV
			R_L = 2 kΩ		330	400	mV
		V_S = +4.5V	R_L = 10 kΩ		10	20	mV
			R_L = 2 kΩ		40	50	mV
	Over temperature	V_S = +36 V	R_L = 10 kΩ		105	110	mV
			R_L = 2 kΩ		480	530	mV
		V_S = +4.5 V	R_L = 10 kΩ		15	20	mV
			R_L = 2 kΩ		55	70	mV
I_{SC}	Short-circuit current				+75/–75		mA
C_{LOAD}	Capacitive load drive				See Typical Characteristics		pF
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			60		Ω
POWER SUPPLY							
V_S	Specified voltage range			+4.5		+36	V
I_Q	Quiescent current per amplifier	I_O = 0 A			1.6	1.8	mA
	Over temperature	I_O = 0 A, T_A = –40°C to +125°C				2	mA
TEMPERATURE							
	Specified range			–40		+125	°C
	Operating range			–55		+150	°C

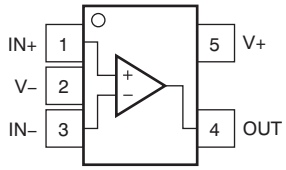
THERMAL INFORMATION: OPA172

THERMAL METRIC[1]		OPA172			UNITS
		D (SO)	DBV (SOT23)	DCK (SC-70)	
		8 PINS	5 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	126.5	227.9	285.2	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	80.6	115.7	60.5	
θ_{JB}	Junction-to-board thermal resistance	67.1	65.9	78.9	
ψ_{JT}	Junction-to-top characterization parameter	31.0	10.7	0.8	
ψ_{JB}	Junction-to-board characterization parameter	66.6	65.3	77.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	

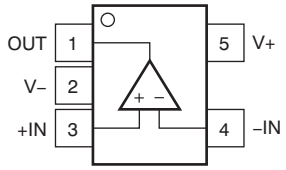
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATIONS

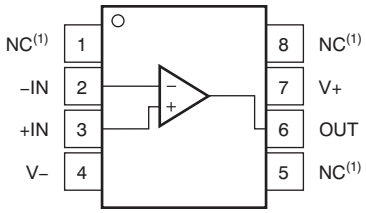
DCK PACKAGE: OPA172
SC-70
(TOP VIEW)



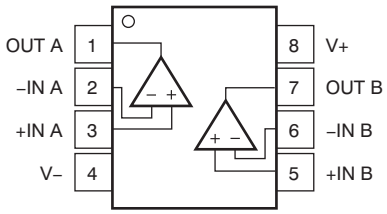
DBV PACKAGE: OPA172
SOT23-5
(TOP VIEW)



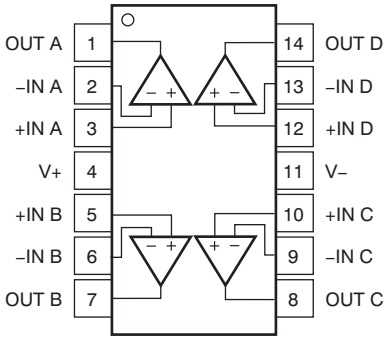
D PACKAGE: OPA172
SO-8
(TOP VIEW)



D AND DGK PACKAGES: OPA2172
SO-8 AND MSOP-8
(TOP VIEW)



D AND PW PACKAGES: OPA4172
SO-14 AND TSSOP-14
(TOP VIEW)



(1) No internal connection.

NOTE: OPA172 D package is production data. All other packages are product preview.

TYPICAL CHARACTERISTICS: TABLE OF GRAPHS

Table 1. List of Typical Characteristics

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution	Figure 2
Offset Voltage vs Temperature (V_S = ±18 V)	Figure 3
Offset Voltage vs Common-Mode Voltage (V_S = ±18 V)	Figure 4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	Figure 5
Offset Voltage vs Power Supply	Figure 6
I_B vs Common-Mode Voltage	Figure 7
Input Bias Current vs Temperature	Figure 8
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 9
CMRR and PSRR vs Frequency (Referred-to Input)	Figure 10
CMRR vs Temperature	Figure 11
PSRR vs Temperature	Figure 12
0.1-Hz to 10-Hz Noise	Figure 13
Input Voltage Noise Spectral Density vs Frequency	Figure 14
THD+N Ratio vs Frequency	Figure 15
THD+N vs Output Amplitude	Figure 16
Quiescent Current vs Temperature	Figure 17
Quiescent Current vs Supply Voltage	Figure 18
Open-Loop Gain and Phase vs Frequency	Figure 19
Closed-Loop Gain vs Frequency	Figure 20
Open-Loop Gain vs Temperature	Figure 21
Open-Loop Output Impedance vs Frequency	Figure 22
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 23, Figure 24
Positive Overload Recovery	Figure 25, Figure 26
Negative Overload Recovery	Figure 27, Figure 28
Small-Signal Step Response (10 mV)	Figure 29, Figure 30
Small-Signal Step Response (100 mV)	Figure 31, Figure 32
Large-Signal Step Response (1 V)	Figure 33, Figure 34
Large-Signal Settling Time (10-V Positive Step)	Figure 35
Large-Signal Settling Time (10-V Negative Step)	Figure 36
No Phase Reversal	Figure 37
Short-Circuit Current vs Temperature	Figure 38
Maximum Output Voltage vs Frequency	Figure 39
EMIRR vs Frequency	Figure 40

TYPICAL CHARACTERISTICS

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

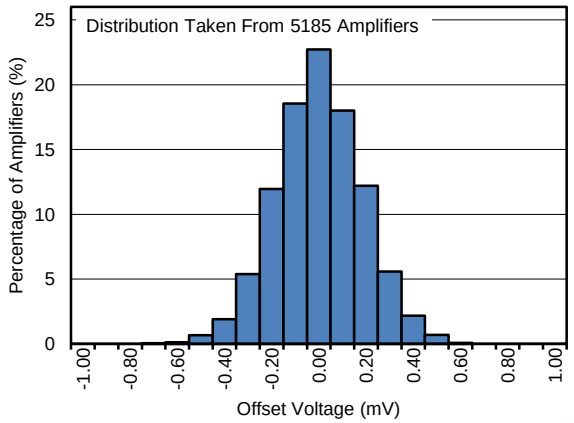


Figure 1. OFFSET VOLTAGE PRODUCTION DISTRIBUTION

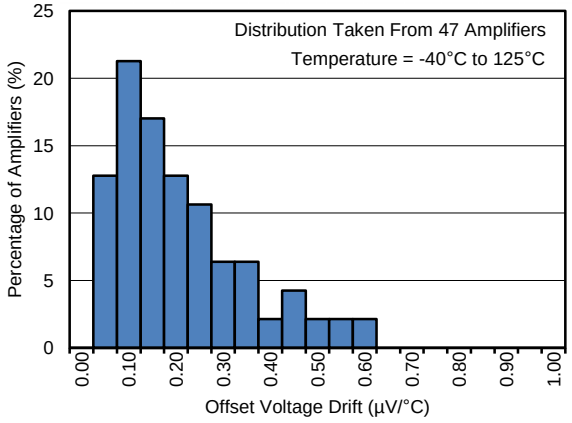


Figure 2. OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

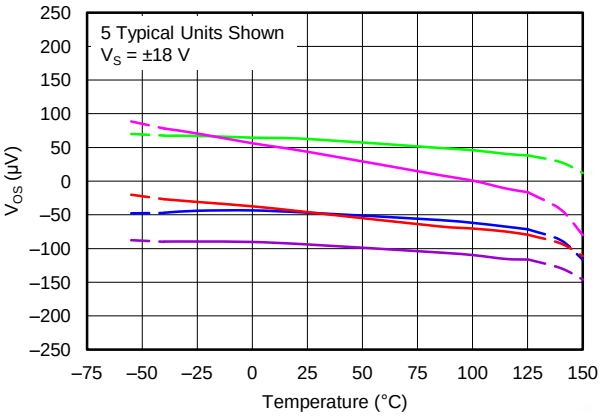


Figure 3. OFFSET VOLTAGE vs TEMPERATURE (V_S = ±18 V)

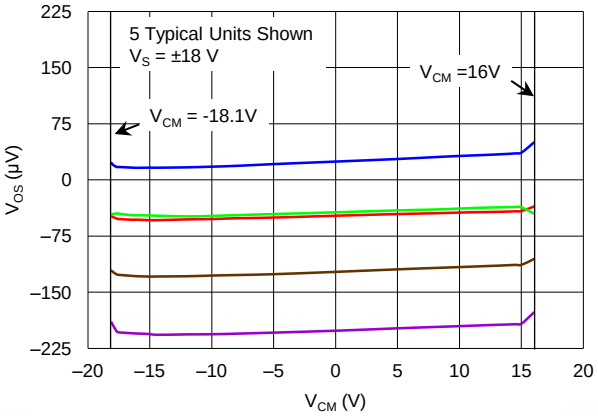


Figure 4. OFFSET VOLTAGE vs COMMON-MODE VOLTAGE (V_S = ±18 V)

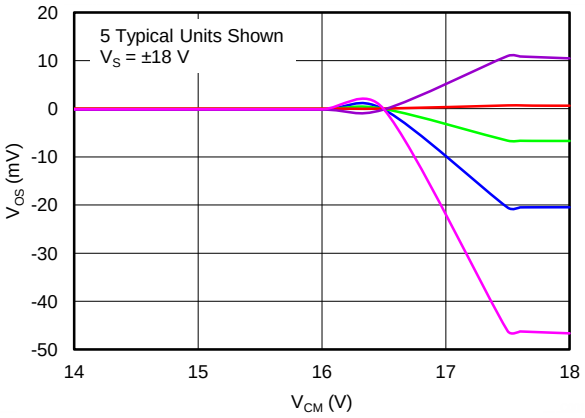


Figure 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

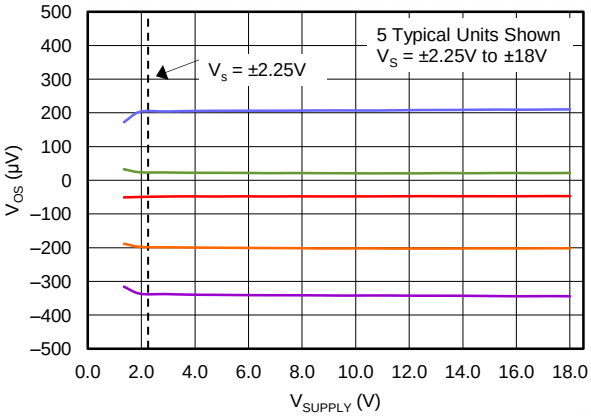


Figure 6. OFFSET VOLTAGE vs POWER SUPPLY

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

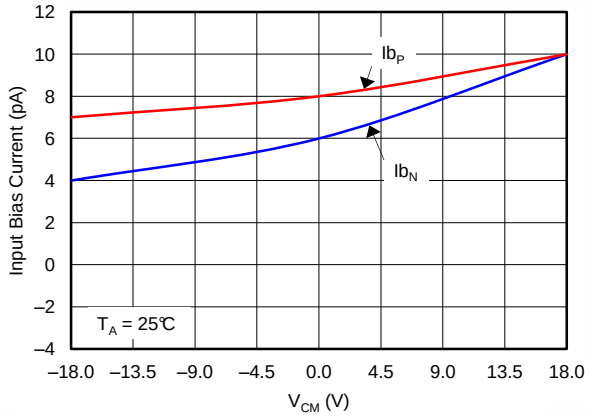


Figure 7. INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

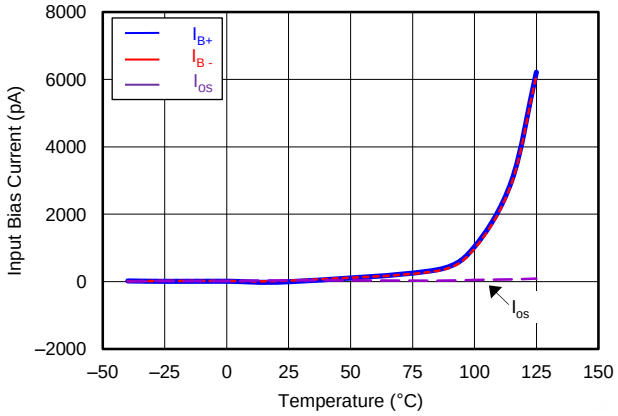


Figure 8. INPUT BIAS CURRENT vs TEMPERATURE

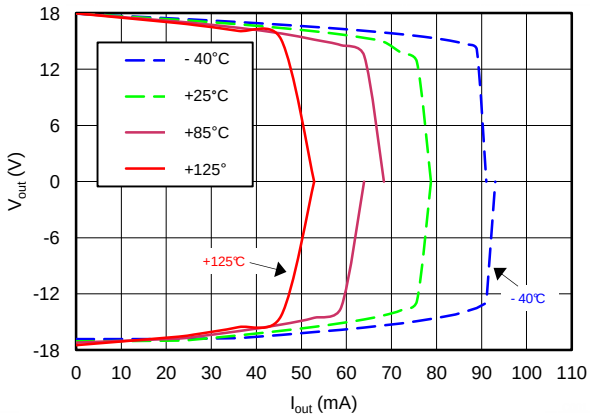


Figure 9. OUTPUT VOLTAGE SWING vs OUTPUT CURRENT (Maximum Supply)

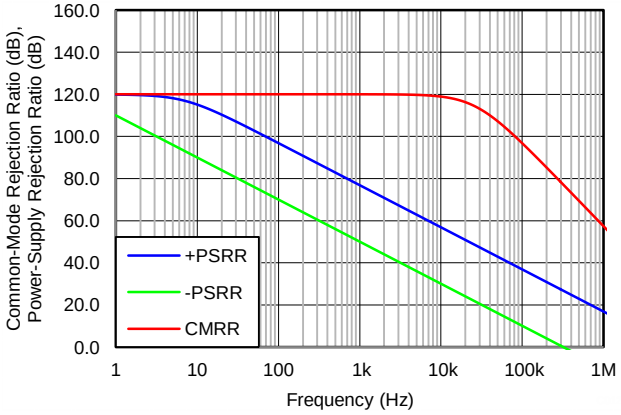


Figure 10. CMRR AND PSRR vs FREQUENCY (Referred-to-Input)

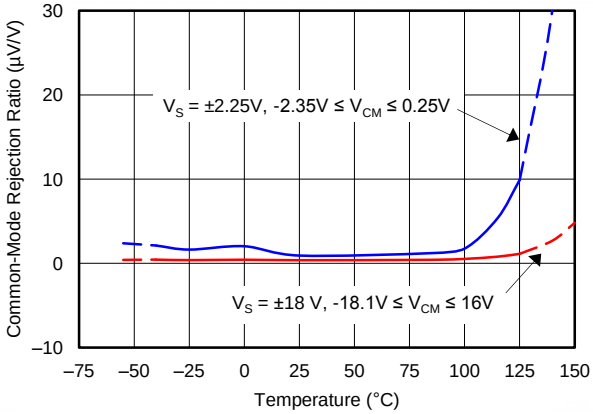


Figure 11. CMRR vs TEMPERATURE

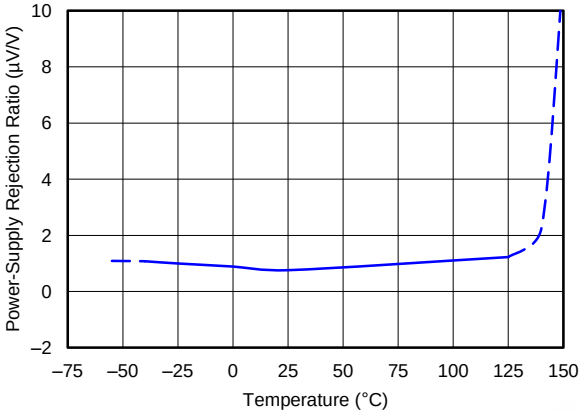


Figure 12. PSRR vs TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

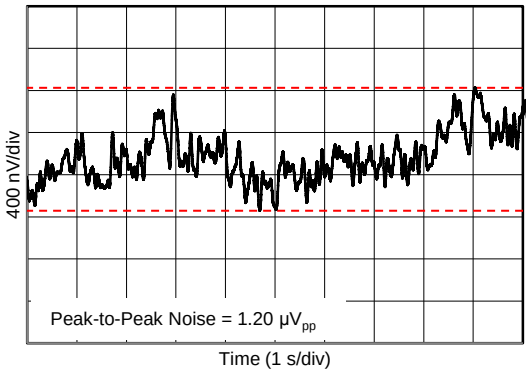


Figure 13. 0.1-Hz TO 10-Hz NOISE

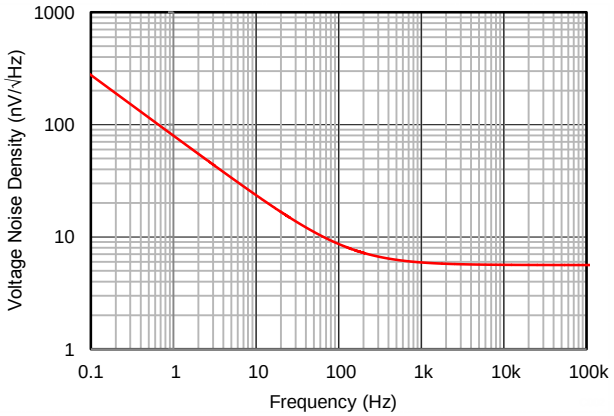


Figure 14. INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

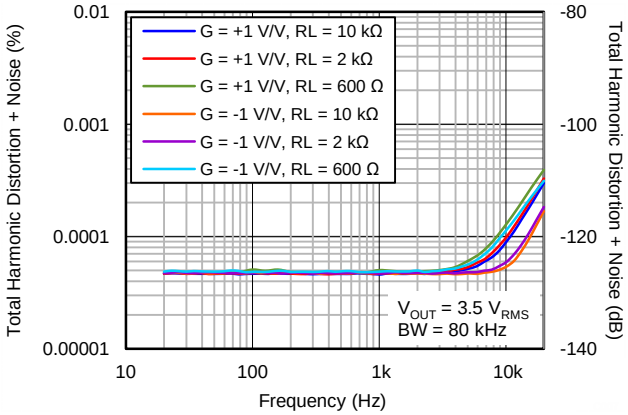


Figure 15. THD+N RATIO vs FREQUENCY

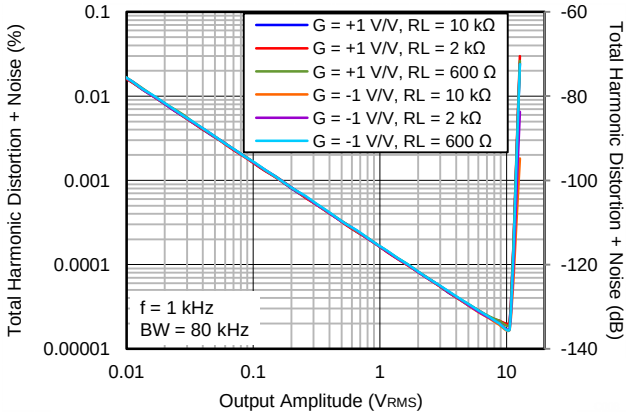


Figure 16. THD+N vs OUTPUT AMPLITUDE

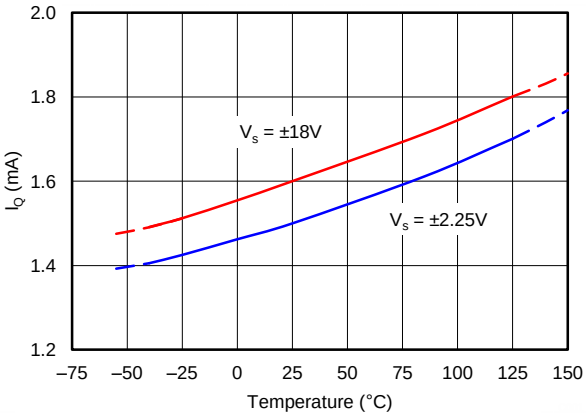


Figure 17. QUIESCENT CURRENT vs TEMPERATURE

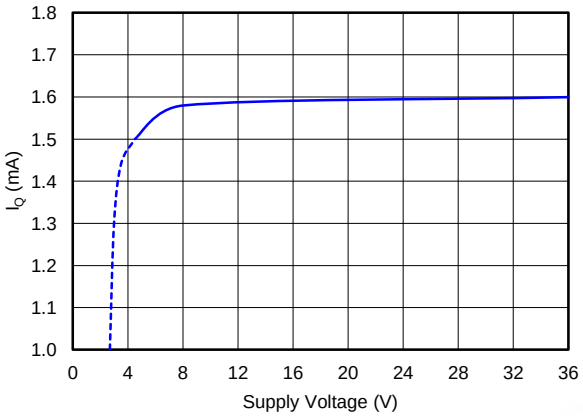


Figure 18. QUIESCENT CURRENT vs SUPPLY VOLTAGE

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

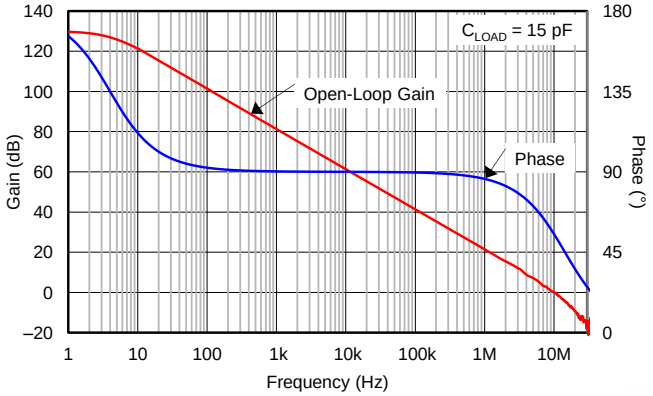


Figure 19. OPEN-LOOP GAIN AND PHASE vs FREQUENCY

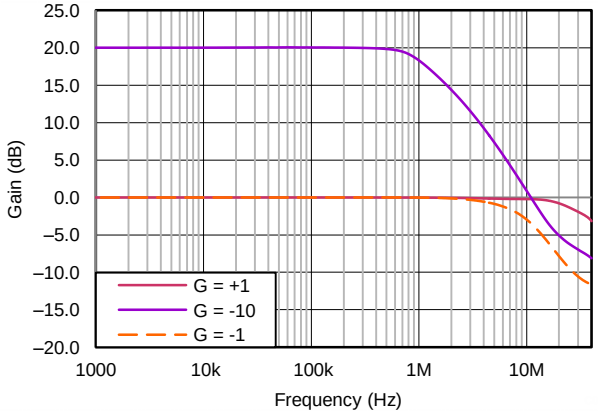


Figure 20. CLOSED-LOOP GAIN vs FREQUENCY

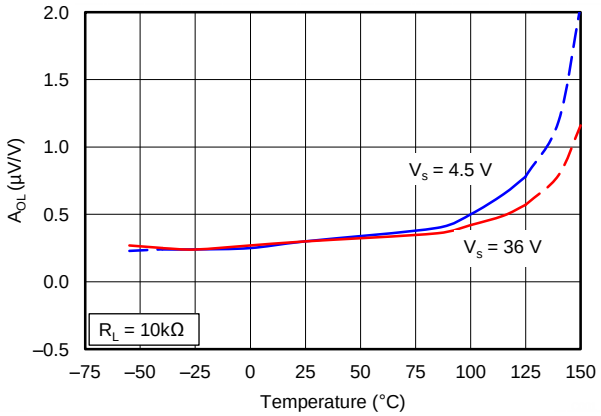


Figure 21. OPEN-LOOP GAIN vs TEMPERATURE

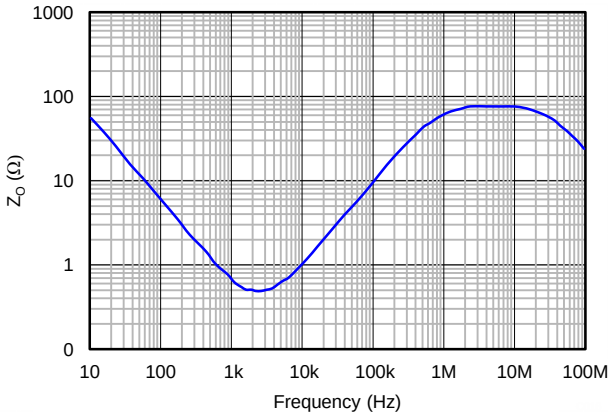


Figure 22. OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

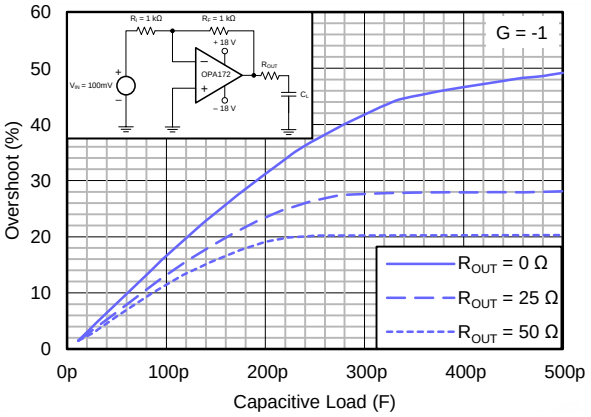


Figure 23. SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100-mV Output Step)

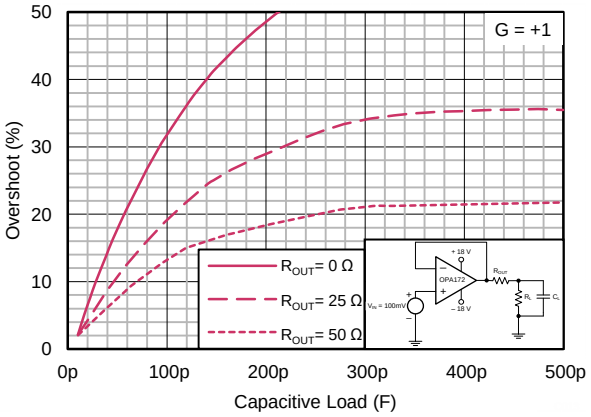


Figure 24. SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100-mV Output Step)

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

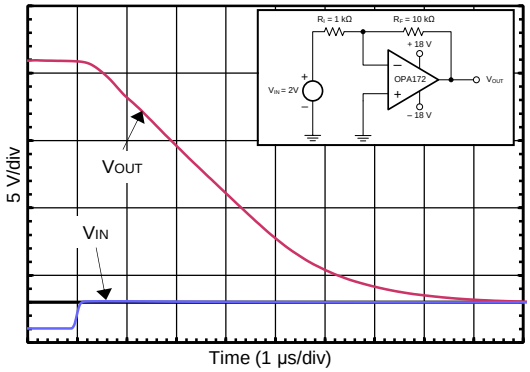


Figure 25. POSITIVE OVERLOAD RECOVERY

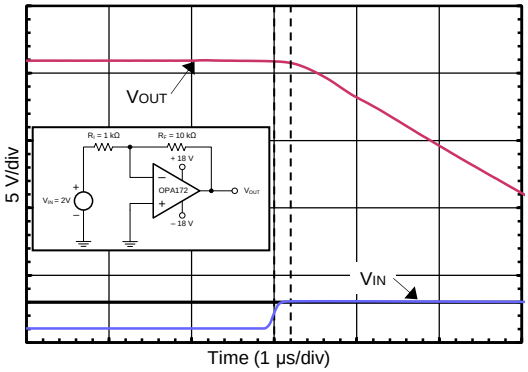


Figure 26. POSITIVE OVERLOAD RECOVERY (Zoomed In)

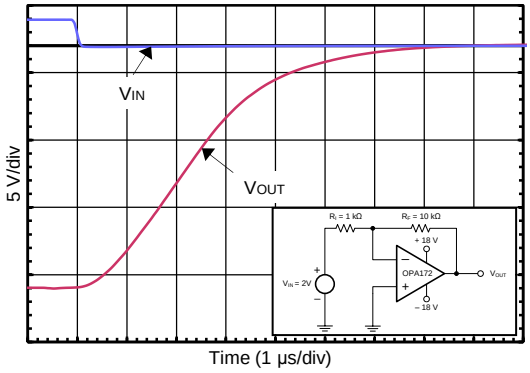


Figure 27. NEGATIVE OVERLOAD RECOVERY

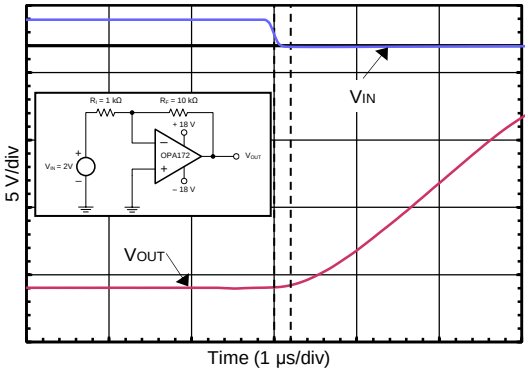


Figure 28. NEGATIVE OVERLOAD RECOVERY (Zoomed In)

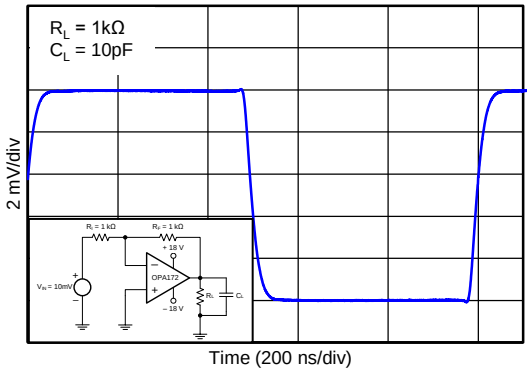


Figure 29. SMALL-SIGNAL STEP RESPONSE (10 mV, G = –1)

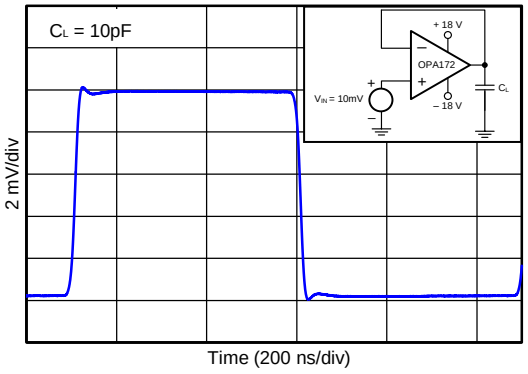


Figure 30. SMALL-SIGNAL STEP RESPONSE (10 mV, G = +1)

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

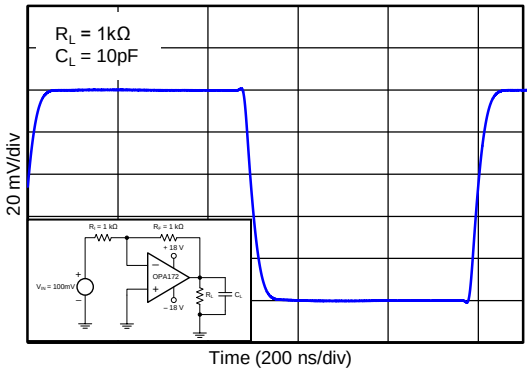


Figure 31. SMALL-SIGNAL STEP RESPONSE (100 mV, G = –1)

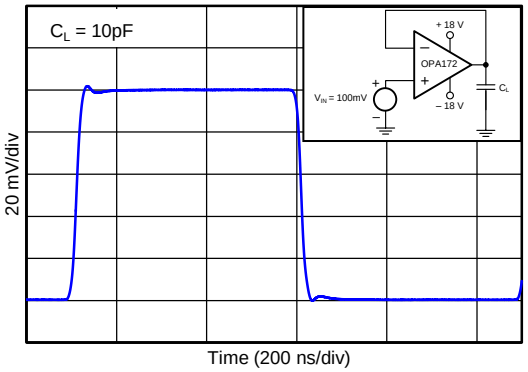


Figure 32. SMALL-SIGNAL STEP RESPONSE (100 mV, G = +1)

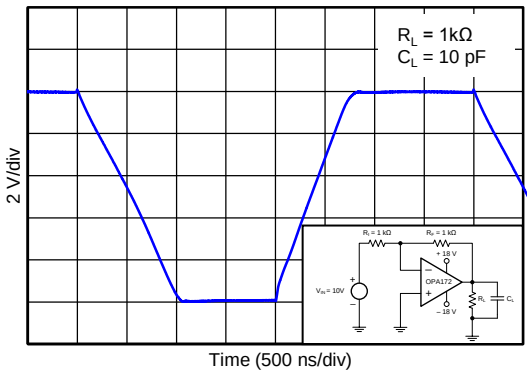


Figure 33. LARGE-SIGNAL STEP RESPONSE (10 V, G = –1)

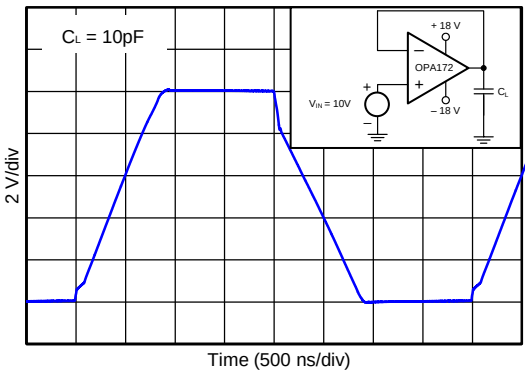


Figure 34. LARGE-SIGNAL STEP RESPONSE (10 V, G = +1)

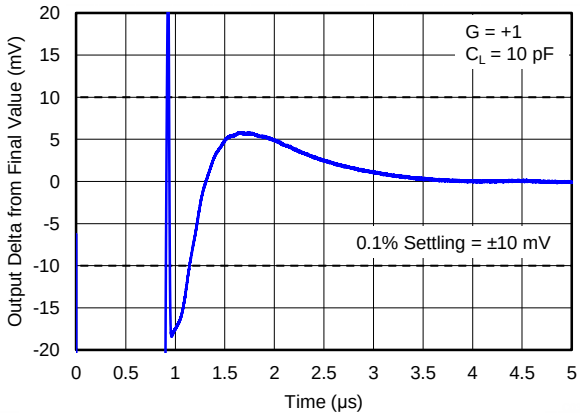


Figure 35. LARGE-SIGNAL SETTLING TIME (10-V Positive Step)

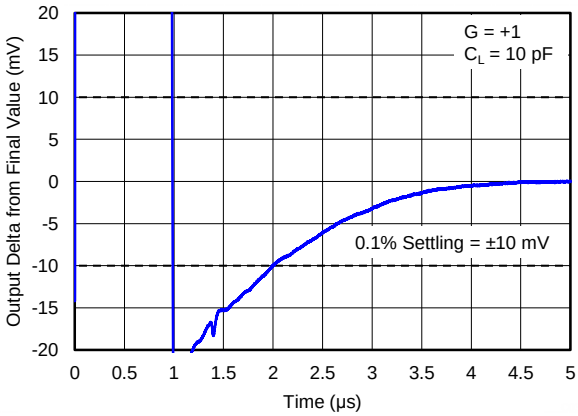


Figure 36. LARGE-SIGNAL SETTLING TIME (10-V Negative Step)

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

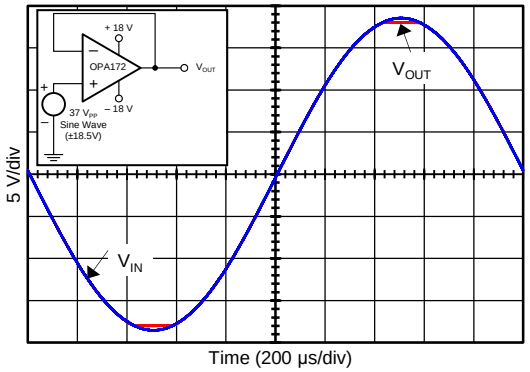


Figure 37. NO PHASE REVERSAL

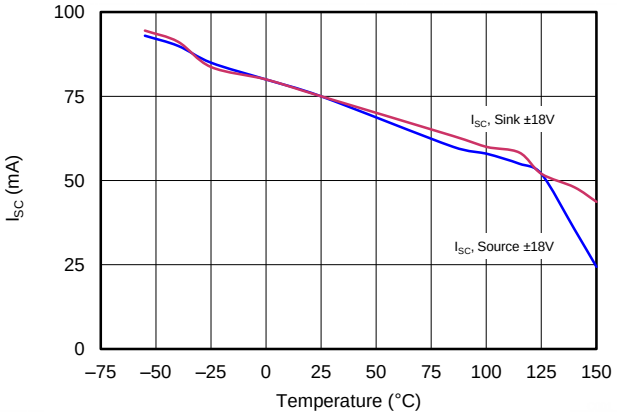


Figure 38. SHORT-CIRCUIT CURRENT vs TEMPERATURE

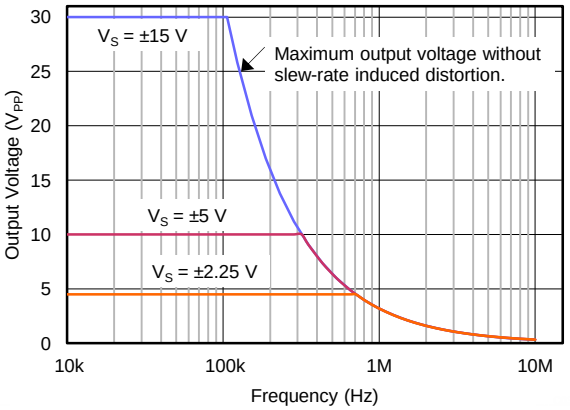


Figure 39. MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

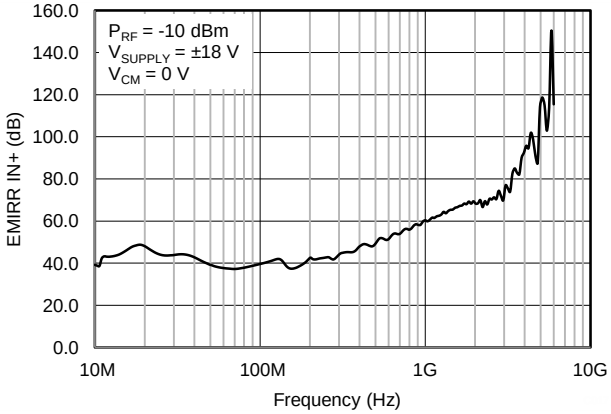


Figure 40. EMIRR vs FREQUENCY

APPLICATION INFORMATION

The OPAx172 family of operational amplifiers provide high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only 1.5 µV/°C (max) provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, A_{OL} and THD.

OPERATING CHARACTERISTICS

The OPAx172 family of amplifiers is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

EMI REJECTION

The OPAx172 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx172 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 41 shows the results of this testing on the OPAx172. Table 2 shows the EMIRR IN+ values for the OPAx172 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 2 can be centered on or operated near the particular frequency shown. Detailed information can also be found in Application Report SBOA128, *EMI Rejection Ratio of Operational Amplifiers*, available for download from www.ti.com.

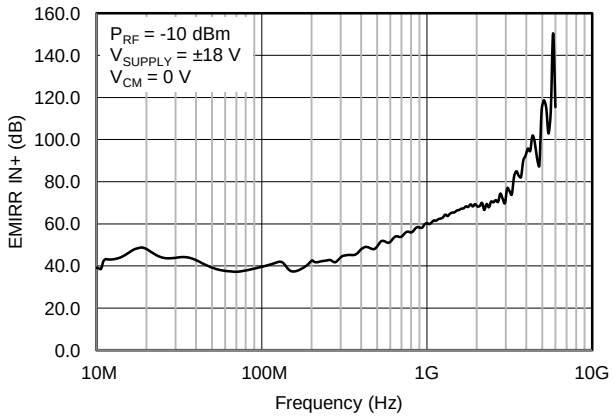


Figure 41. EMIRR Testing

Table 2. OPAx172 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh frequency (UHF) applications	47.6 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	58.5 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	68 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	69.2 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	82.9 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	114 dB

GENERAL LAYOUT GUIDELINES

For best operational performance of the device, good printed circuit board (PCB) layout practices are recommended. Including:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.
- In order to reduce parasitic coupling, run the input traces as far away from the supply lines as possible.
- A ground plane helps distribute heat and reduces EMI noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

COMMON-MODE VOLTAGE RANGE

The input common-mode voltage range of the OPAx172 series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in Table 3.

Table 3. Typical Performance Range (V_S = ±18V)

PARAMETER	MIN	TYP	MAX	UNIT
Input Common-Mode Voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		5		mV
vs Temperature (T_A = –40°C to +125°C)		10		µV/°C
Common-mode rejection		70		dB
Open-loop gain		60		dB
GBW		4		MHz
Slew rate		4		V/µs
Noise at f = 1 kHz		22		nV/√Hz

PHASE-REVERSAL PROTECTION

The OPAx172 family has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx172 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 42.

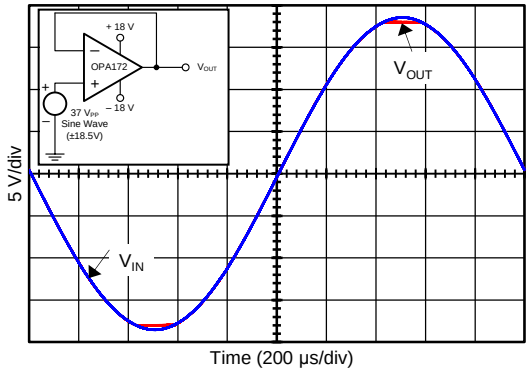


Figure 42. No Phase Reversal

CAPACITIVE LOAD AND STABILITY

The dynamic characteristics of the OPAx172 have been optimized for commonly-encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} = 50 Ω) in series with the output. Figure 43 and Figure 44 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, refer to Application Bulletin SBOA015 (AB-028), *Feedback Plots Define Op Amp AC Performance*, available for download from www.ti.com, for details of analysis techniques and application circuits.

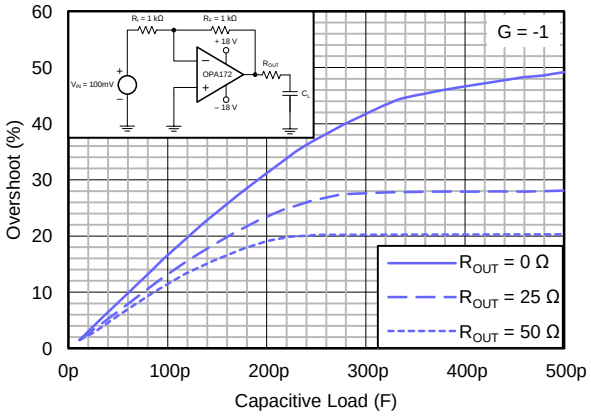


Figure 43. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

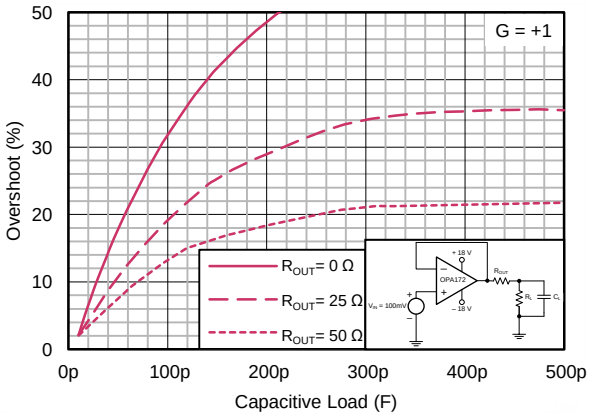


Figure 44. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See Figure 45 for an illustration of the ESD circuits contained in the OPAx172 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

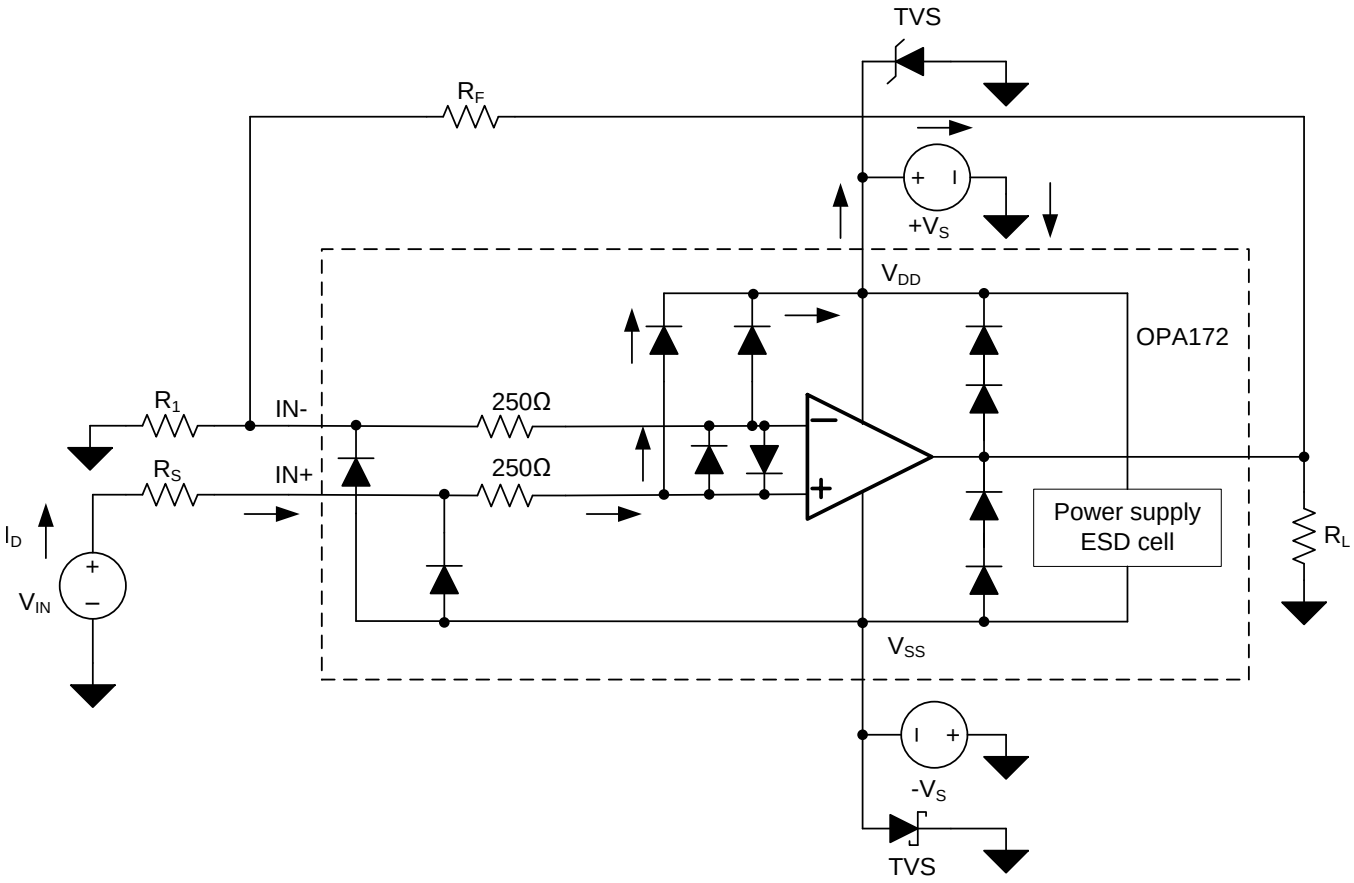


Figure 45. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx172 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (such as the one Figure 45 depicts), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 45 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input-signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current can be supplied by the input source through the current-steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external zener diodes to the supply pins, as shown in Figure 45. Select the zener voltage so that the diode does not turn on during normal operation. However, the zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The OPAx172 input terminals are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 45. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the OPAx172. Figure 45 shows an example configuration that implements a current-limiting feedback resistor.

OVERLOAD RECOVERY

Overload recovery is defined as the time it takes for the op amp output to recover from the saturated state to the linear state. The output devices of the op amp enter the saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx172 is approximately 200 ns.

APPLICATION EXAMPLES

The following application examples highlight only a few of the circuits where the OPAx172 can be used.

BI-DIRECTIONAL CURRENT SOURCE

The improved Howland current pump topology shown in Figure 46 provides excellent performance due to the extremely tight tolerances of the on chip resistors of the INA132. By buffering the output using and OPA172, the output current the circuit is able to deliver is greatly extended.

The circuit dc transfer function is show in Equation 1:

$$I_{OUT} = V_{IN} / R_1 \quad (1)$$

The OPA172 can also be used as the feedback amplifier because the low bias current will minimize error voltages produced across R1. However, for improved performance, a FET-input device with extremely low offset can be selected, such as the OPA192, OPA140, or OPA188 for the feedback amplifier.

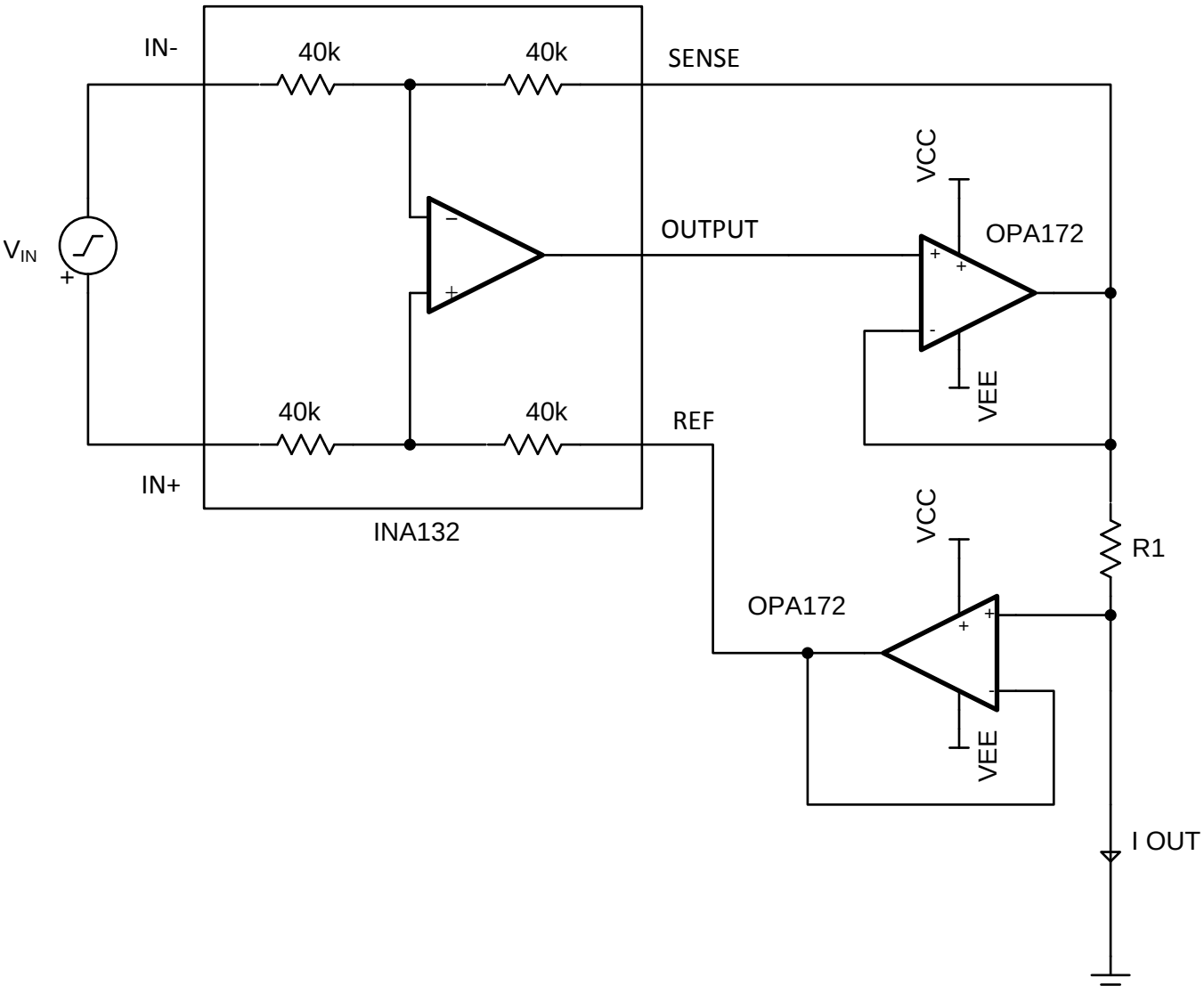


Figure 46. Bidirectional Current Source

JFET-INPUT LOW-NOISE AMPLIFIER

A low-noise composite amplifier can be built adding a low noise JFET pair (Q1 and Q2) as an input preamplifier for the OPA172 as shown in Figure 47. Transistors Q3 and Q4 form a 2-mA current sink that biases each JFET with 1 mA of drain current. Using 3.9-kΩ drain resistors produces a gain of approximately 10 in the input amplifier, making the extremely-low, broadband-noise spectral density of the LSK489 the dominant noise source of the amplifier. The output impedance of the input differential amplifier is large enough that a FET-input amplifier such as the OPA172 provides superior noise performance over bipolar-input amplifiers.

The gain of the composite amplifier is given by Equation 2:

$$A_V = (1 + R_3 / R_4) \quad (2)$$

The resistances shown are standard 1% resistor values that produce a gain of approximately 100 (99.26) with 68° of phase margin. Gains less than 10 may require additional compensation methods to provide stability. Seleect low resistor values to minimize the resistor thermal noise contribution to the total output noise.

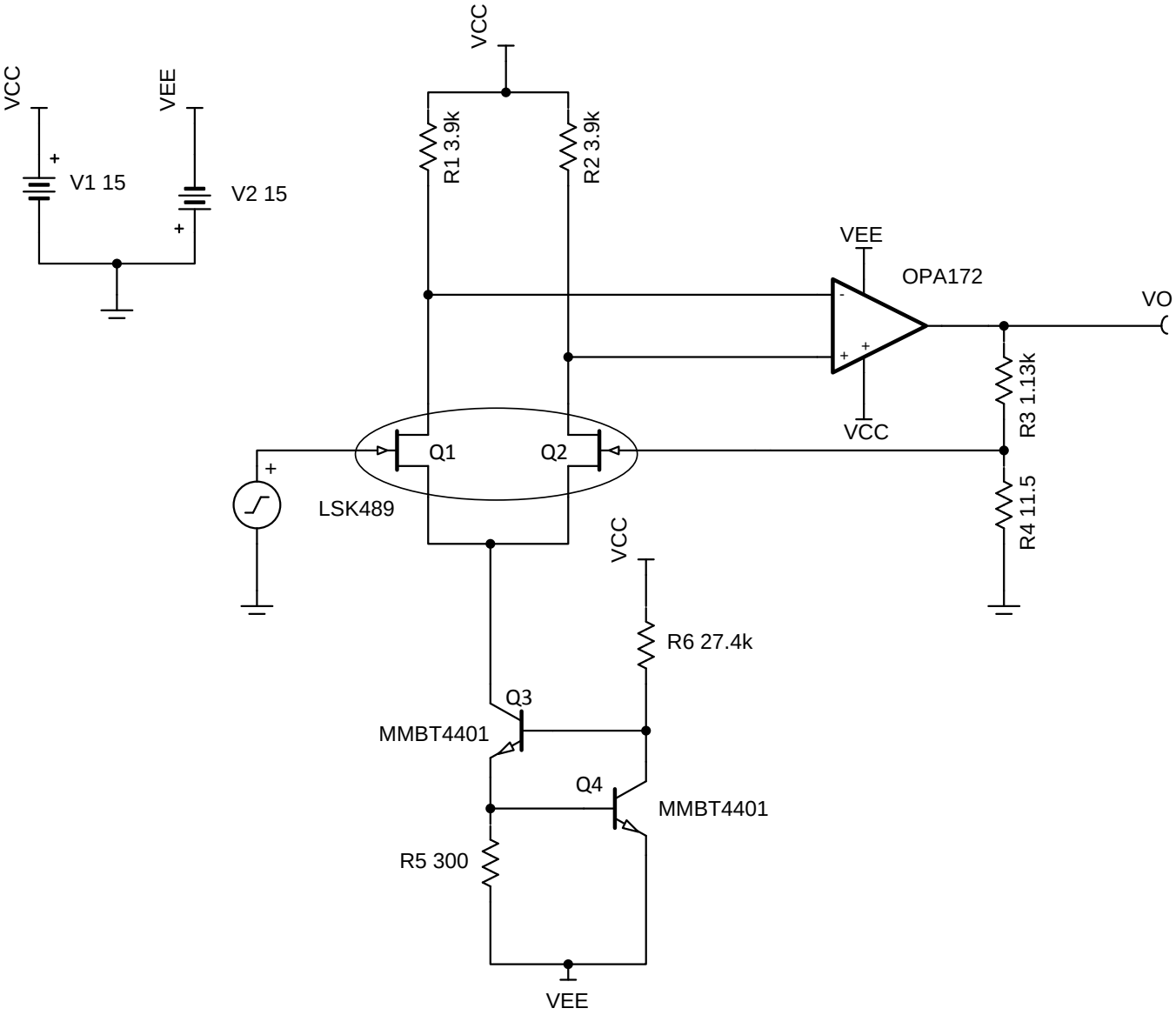


Figure 47. JFET-Input Low-Noise Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA172ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA172	Samples
OPA172IDBVR	PREVIEW	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUWQ	
OPA172IDBVT	PREVIEW	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUWQ	
OPA172IDCKR	PREVIEW	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIU	
OPA172IDCKT	PREVIEW	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIU	
OPA172IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA172	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

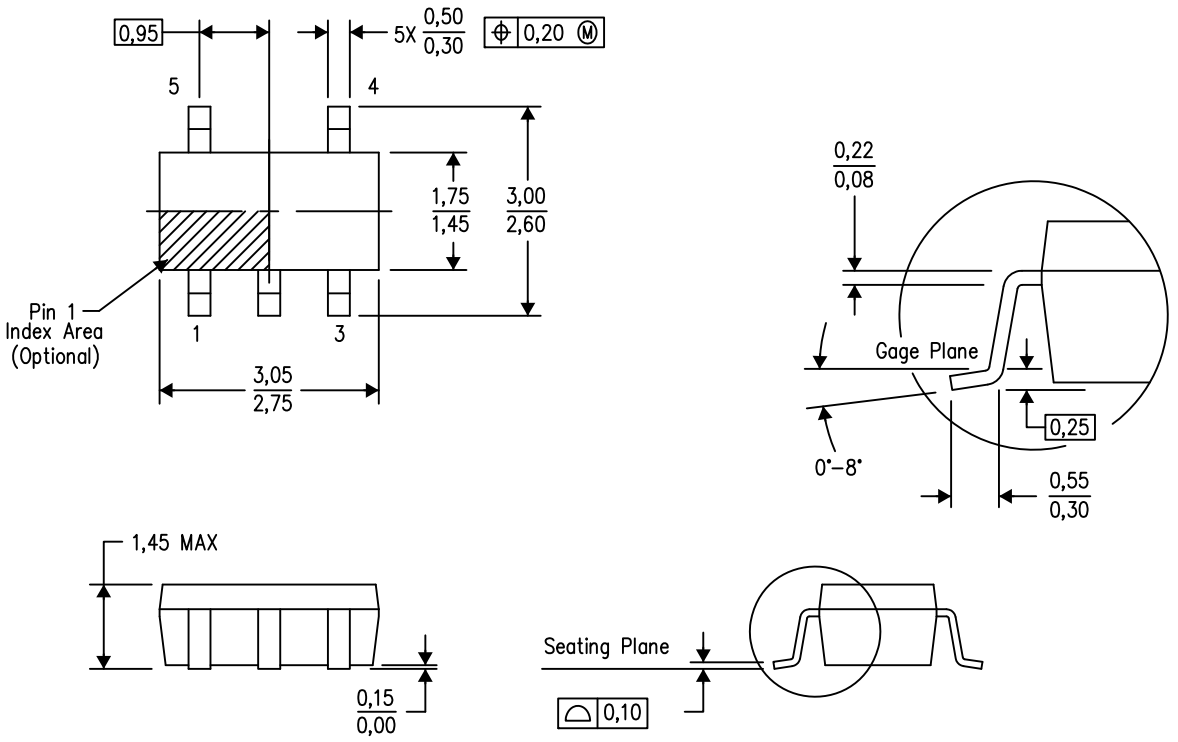
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

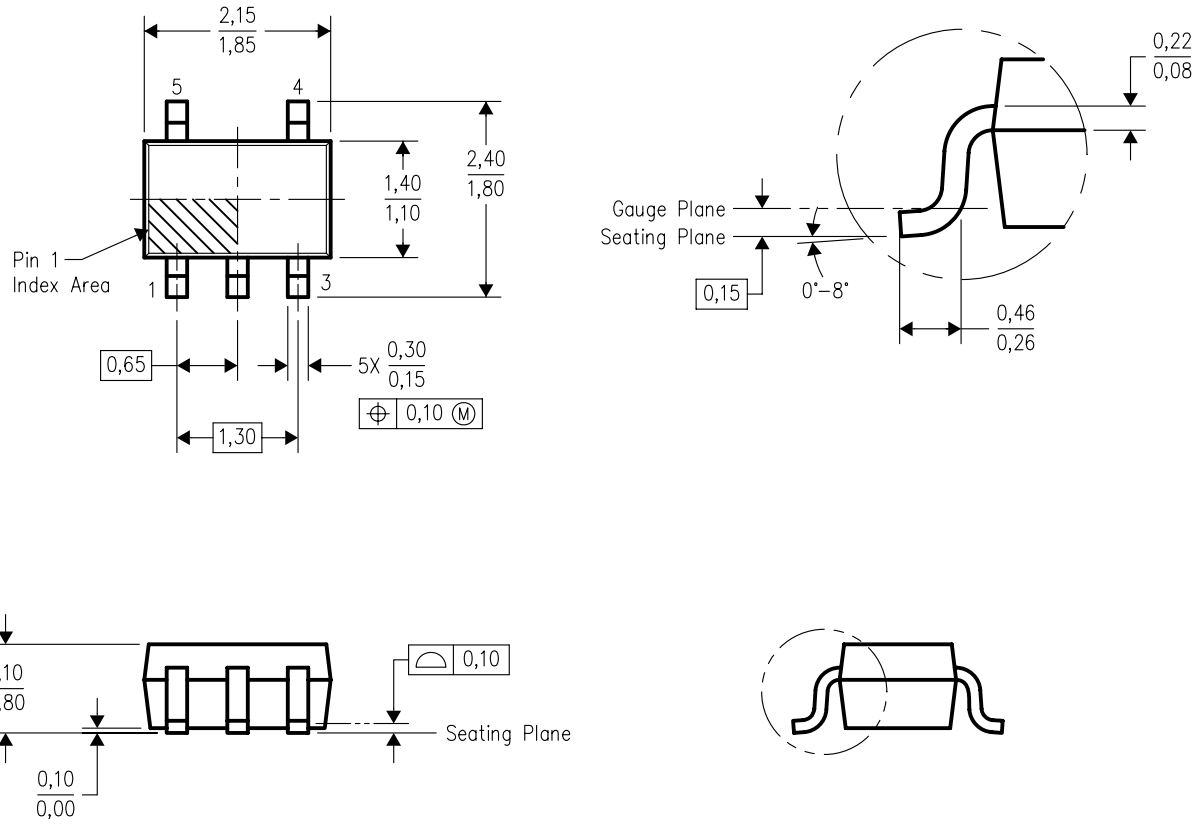
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

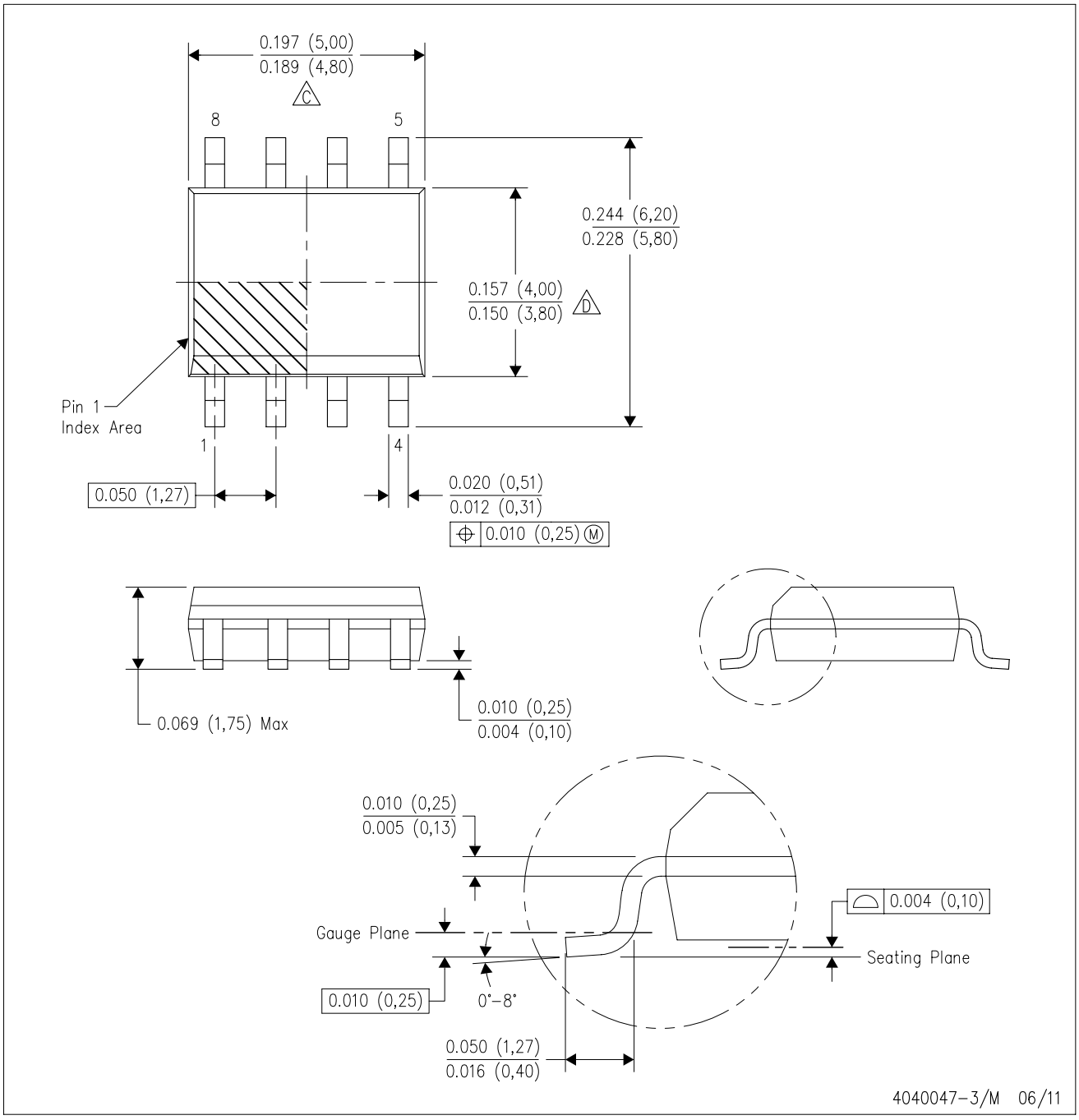
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

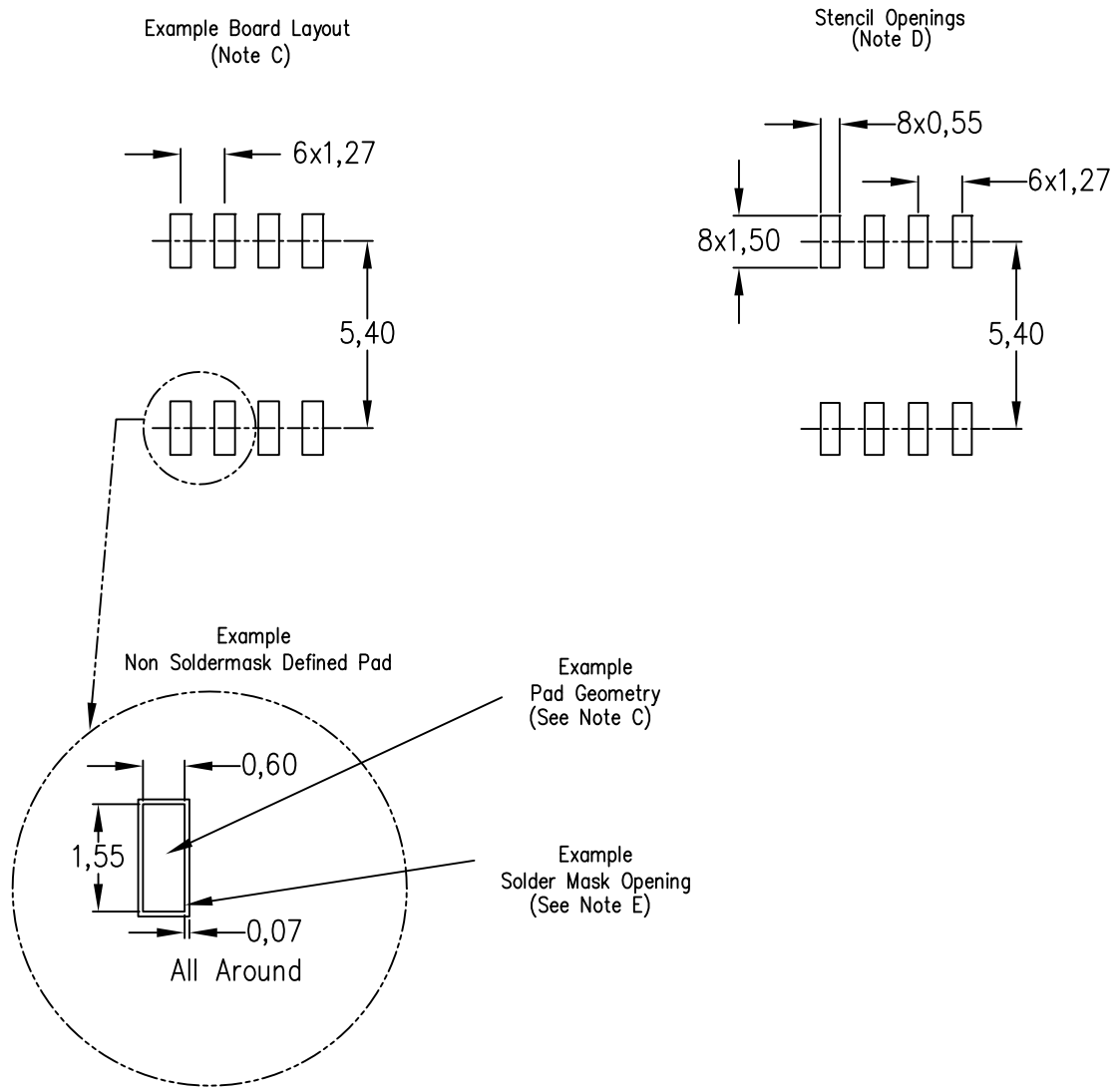
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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